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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Complete if Known	
				Application Number	09/656,763
				Filing Date	September 7, 2000
				First Named Inventor	Lin Wu
				Group Art Unit	2632
				Examiner Name	Not Yet Assigned
				Attorney Docket Number	19000.0045/P045
Sheet	1	of			

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Examiner Signature		Date Considered	
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Unique citation designation number. ² See attached Kinds of U.S. Patent Documents. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the application number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.



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Sheet	2	of		

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OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials [*]	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, Application, symposium, catalog, etc), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
HN	A	JOHN G. MANEATIS, "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques", <i>IEEE Journal of Solid-State Circuits</i> , Vol. 31, No. 11, November 1996, pages 1723-1732.	
HN	B	CHAN-HONG PARK et al., "A Low-Noise, 900-MHz VCO in 0.6- μ m CMOS", <i>IEEE Journal of Solid-State Circuits</i> , Vol. 34, No. 5, May 1999, pages 586-591.	
HN	C	ALI HAJIMIRI et al., "Jitter and Phase Noise in Ring Oscillators", <i>IEEE Journal of Solid-State Circuits</i> , Vol. 34, No. 6, June 1999, pages 790-804.	
HN	D	BEOMSUP KIM et al., "PLL/DLL System Noise Analysis for Low Jitter Clock Synthesizer Design", <i>Department of Electrical Engineering and Computer Sciences, University of California, Berkley / Department of Electrical Engineering, Korea Advanced Institute of Science and Technology</i> , pages 31-34.	
HN	E	JOHN A. MCNEILL, "Jitter in Ring Oscillators", <i>IEEE Journal of Solid-State Circuits</i> , Vol. 32, No. 6, June 1997, pages 870-879.	
HN	F	BEHZAD RAZAVI, "A Study of Phase Noise in CMOS Oscillators", <i>IEEE Journal of Solid-State Circuits</i> , Vol. 31, No. 3, March 1996, pages 331-343.	
HN	G	RICHARD GU et al., "A 0.5-3.5Gb/s Low-Power Low-Jitter Serial Data CMOS Transceiver", 1999 <i>IEEE International Solid-State Circuits Conference</i> , ISSCC99/Session 20/Paper WA 20.4, pages 352-353 and 478.	
HN	H	JOONSUK LEE et al., "A 250MHz Low Jitter Adaptive Bandwidth PLL", 1999 <i>IEEE International Solid-State Circuits Conference</i> , ISSCC99/Session 20/Paper WA 20.1, pages 346346-347 and 477.	
HN	I	DAVID W. BOERSTLER, "A Low-Jitter PLL Clock Generator for Microprocessors with Lock Range of 340-612 MHz", <i>IEEE Journal of Solid-State Circuits</i> , Vol. 34, No. 4, April 1999, pages 513-519.	

Examiner Signature	HAI L. NGUYEN	Date Considered	6/25/01
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HEN	A	T. SAEKI, et al., "A 1.3 cycle lock time, non PLL/DLL jitter suppression clock multiplier based on direct clock cycle interpolation for 'Clock on Demand'", 2000 IEEE International Solid-State Circuits Conference (2000), p. 166-167.	
HEN	B	I. HWANG, et al., "A digitally controlled phase-locked loop with fast locking scheme for clock synthesis application", 2000 IEEE International Solid-State Circuits Conference (2000), p. 168-169.	

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First Named Inventor	Lin Wu
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Sheet	1	of	2
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U.S. PATENT DOCUMENTS

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